IN THE CLAIMS

1. (Currently Amended) A method for aliasing stacked registers of a register file of a processor ~~aliasing~~ within a data hazard detection circuit of [a] the processor to reduce dependency of the data hazard detection circuit upon size of the register file, comprising the steps of:

identifying a first group of consecutive registers within [a] the register file ~~of the processor~~;

aliasing the first group of registers to ~~first~~ a group of register identifiers within the data hazard detection circuit;

detecting data hazards, if any, associated with the ~~first~~ group of register identifiers;

identifying a second group of consecutive registers within the register file, the first and second group of registers not overlapping;

aliasing the second group of consecutive registers to ~~second~~ the group of register identifiers; and

detecting, within the data hazard detection circuit, data hazards, if any, associated with the ~~second~~ group of register identifiers~~, wherein the first and second register identifiers overlap in hazard detect logic across two or more rows of the register file~~.

2. (Previously Presented) The method of claim 1, each of the steps of identifying comprising identifying registers within a 128-register register file.

3. (Previously Presented) The method of claim 2, the steps of detecting comprising utilizing groups of 32 register identifiers to alias data hazard detect logic to windows of 32-register frames.

4. (Currently Amended) A processor for processing program instructions, comprising:

a register file grouped into two or more non-overlapping equally sized groups ~~stacks~~ of consecutive registers;

an execution unit having an array of pipelines for processing the instructions and for writing bypass data to the register file; and

a data hazard detection circuit ~~logic~~ for detecting data hazards in the bypass data without differentiation between corresponding registers of each ~~stack~~ group.

5. (Currently Amended) The processor of claim 4, further comprising a register ID file ~~for facilitating data hazard detection, the register ID file~~ having a plurality of register identifiers, the data hazard detection circuit ~~logic~~ aliasing data hazard detection according to mapping of ~~the~~ each register identifier[s] to a corresponding register[s] of each ~~stack~~ group of consecutive registers.

6. (Currently Amended) The processor of claim 5, the register ID file mapping sequential 32-registers within the ~~common~~ data hazard detection circuit ~~logic~~ to more than 32 registers of the register file to alias in 32-register sequences.

7. (Currently Amended) In a data hazard detection circuit ~~logic~~ of a processor of the type having a register file and a register ID file providing row-to-row data hazard detection, the improvement wherein each register ID of the register ID file aliases row-to-row hazard detection of the register file ~~by common~~ within the data hazard detection ~~logic~~ circuit for two or more non-consecutive rows of the register file, thereby identifying data hazards, if any, and reducing dependency of the data hazard detection circuit upon size of the register file.

8. (Currently Amended) A method for data hazard detection within a processor of the type having a register file, a register ID file and a data hazard detection circuit, comprising:

aliasing each register identifier of a group of register identifiers of the register ID file to two or more registers of [a] the register file ~~of the processor~~, the register file formed of equally sized non-overlapping groups of consecutive registers, each of the register identifiers aliasing one corresponding register of each group of registers; and

determining data hazards within the register file by comparing one or more of the register identifiers within the data hazard detection circuit.

9-10. (Cancelled)

11. (Currently Amended) The method of claim 8, wherein the step of aliasing increases the register file size without a corresponding increase in data hazard detection ~~logic~~ circuit.

12. (Previously Presented) The method of claim 8, wherein the group of register identifiers has 32 register identifiers.

13. (Currently Amended) A method of reducing dependency of a data hazard ~~logic dependency~~ detection circuit within a processor on size of a register file within [a] the processor, comprising:

selecting a register ID file size;

aliasing at least one entry of the register ID file to two or more registers of the register file, each of the two or more registers being located in a non-overlapping group of sequential registers equivalent in size to the selected register ID file size; and

evaluating matches between entries of the register ID file in the hazard logic without distinguishing between common aliased entries of the register file.

14. (Previously Presented) The method of claim 13, wherein the step of aliasing increases the register file size without a corresponding increase in data hazard detection logic.

15. (Currently Amended) A method of data hazard detection within a processor of the type having a register file, a register ID file and a data hazard detection circuit, comprising:

aliasing each register ID within the data hazard detection ~~logic~~ circuit to two or more non-consecutive registers of [a] the register file; and

determining data hazards by matching register IDs within the data hazard ~~logic~~ detection circuit.

16. (Currently Amended) A method for stacked register aliasing in a data hazard detection ~~logic~~ circuit of a processor, comprising:

aliasing two or more non-overlapping groups of consecutive registers of a stacked register file within the processor to one group of consecutive register IDs within the data hazard detection circuit ~~logic~~, each register ID aliasing one register from each group of consecutive registers; and

detecting data hazards, if any, associated with a first and second register of the stacked register file by comparing a first aliased register ID of the first register to a second aliased register ID of the second register within the data hazard detection ~~logic~~ circuit.

17. (Previously Presented) The method of claim 12, wherein each group of consecutive registers has 32 registers.